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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,945	07/10/2001	Toshitada Saito	211200US2	7956

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,945	SAITO, TOSHITADA	
	Examiner	Art Unit	
	John P. Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the applicant's amendment and RCE dated 3/29/2005.

The applicant amended claims 1 and 2.

Claims 1-12 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/29/2005 has been entered.

Information Disclosure Statement

2. The examiner has considered the Information Disclosure Statement dated 10/28/2004.

Response to Amendment

3. Applicant's arguments, see amendment, filed 3/29/2005, with respect to the rejection of Claim 1 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn, as well as the rejection of

independent Claims 2-12. However, upon further consideration, a new ground of rejection is made in view of the applicant's admitted prior art and Ogino et al. (see below).

Claim Rejections - 35 USC § 103

4. Claims 1, 2- 4 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (herein "APA") published as U.S. Patent Application No. 2002/0026553, in view of Higashida, U.S. Patent No. 6523136, and further in view of Ogino et al., U.S. Patent No. 5416919.

As per Claim 1:

The APA teaches a system LSI (APA FIG.3 50) comprising: a storage circuit (FIG.3 53) in which an operational program (FIG.3 54) and a debug functional program (FIG.3 55) are stored; at least one processor circuit (FIG.3 51) for carrying out a processing operation in accordance with said operation program (paragraph [0003]), a peripheral circuit (FIG.3 56), capable of sending and receiving a signal to and from said processor circuit, for carrying out a predetermined logical operation in accordance with an input signal (paragraph [0004]), said peripheral circuit having at least one functional block (paragraph [0007]), a debug circuit (FIG.3 52) for carrying out a debug to a bug caused by said any operation process, on the basis of said debug functional program which is stored in said storage circuit (paragraph [0006]), but fails to specifically disclose a processor having a program counter and arithmetic and register means, as well as selection and selection control means. But Higashida et al. does teach these features,

wherein is disclosed, said processor circuit (FIG.7 2a) having a program counter, at least one computing unit and at least one register (column 2 lines 53-65 and column 6 lines 3-26), selection means (FIG.8 8c) for optionally selecting one of the outputs of said program counter, said computing unit and said register in said processor circuit, at least one output of said storage circuit, and one of the outputs of a plurality of internal signals in said peripheral circuit including the output of said functional block (column 10 lines 65-67 and column 11 lines 1-53); and selection control means for controlling selection of a result signal from any operation process in any place of said processor circuit, said storage circuit and said peripheral circuit (column 10 lines 54-64). And Higashida et al., in column 3 lines 60-67 and column 4 lines 1-30, the advantage is a means for accurately accessing internal bus signals of an LSI without increasing external pin overhead. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the signal selector and control of Higashida et al. to the LSI debug system of the APA in order to decrease the external pin count of the monitored units within the LSI. But Higashida et al. fails to teach the selection control is based on a selection signal which is supplied from the outside of said system LSI via an external terminal. However, in the analogous art of Ogino et al., this feature is taught, wherein the analogous selection means of Ogino et al. (FIG.3 13) is controlled by an analogous selection control means (FIG.3 24) on the basis of a selection signal (FIG.3 D0, D1) supplied from an outside terminal of the LSI (FIG.3 DATA BUS 15). And in column 2 lines 4-9, the advantage is a means of accessing data from a debug system without requiring any extra test-dedicated terminals. One with

ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply the zero pin count test capability of Ogino et al. to the debug system of the APA and Higashida et al. in order to provide internal debugging without adding pin count to the device.

As per Claim 2:

Claim 2, being dependent on Claim 1 above, is further taught by the Ogino et al., wherein the analogous debug backup circuit (FIG.3 24) has an internal control signal generating portion (FIG.4) for generating an internal control signal (FIG.4 37a-37d) during a processing operation based in the debug functional program in the storage circuit (FIG.4 TEST 30), and said selection means (FIG.3 13) carries out a selecting operation on the basis of said internal signal (FIG.3 25), which is generated by said internal control signal generating portion of said processor circuit (FIG.4), and said selection signal which is supplied from the outside (FIG.4 D0, D1). And in view of the motivation previously stated, the claim is rejected.

As per Claim 3:

Claim 3, dependent on Claim 1 above, further limits the system to have three selection units, the 1st to select one of the program counter, register, storage, or processor, the 2nd to select one of the peripheral circuits, and the 3rd to select one of the 1st or second. Higashida teaches all of these selectors, the 1st in FIG. 2 and column 7 lines 15-30, the 2nd in FIG. 3 under control of TP1 and column 7 lines 55-62, and the 3rd in FIG. 3 under control of TP2 and column 7 lines 62-67. Instead of the storage being selected in the 1st selector as claimed by the applicant, Higashida instead selects the

storage units by way of selector 2, and so is not precisely the same as the Claim 3. In would have been obvious to one with ordinary skill in the art at the time of the invention, motivated to use the same bus for storage as for peripherals, to select the Higashida configuration. The examiner does not see any electrical difference in the drawings between the applicant's or the Hgashida configuration, and believes that the applicant's configuration may be the same. Being electrically the same, the Claim 3 is rejected.

As per Claim 4:

Claim 4, dependent on Claim 3 above, further limits the system to a debug backup circuit that is controlled by the processor, and controls selection of the 1st through 3rd selectors as well as the outside signal. Higashida fully teaches this in FIG. 8, by adding the "Register Circuit" 8c in an embodiment of that patent, which derives control from the processor bus (see column 10, lines 54-67 and column 11, lines 1-54), and selects either under control of the processor or external signal. And in view of the motivation previously stated, the claim is rejected.

As per Claim 10:

Claim 10, dependent on Claim 1 above, is further taught by the APA wherein the system has I/O terminals for sending signals to and from a peripheral device (FIG.3, between 51 and 56). And in view of the motivation previously stated, the claim is rejected.

As per Claim 11:

Claim 11, dependent on Claim 10 above, further limits the I/O terminals to being used for inputting/outputting control and monitor signals. Higashida teaches inputting

controls (column 11 lines 1-54) for multiplex controls, outputting monitor signals is not specifically taught. However, the system of Higashida has the same structure as the applicant's, and therefore, under control of the processor, as in column 7 lines 15-67, the same bus which multiplexes monitor data to the monitor output can under the processor control output the data via the I/O bus. One with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and monitor pins, therefore the Claim 11 is rejected.

As per Claim 12:

Claim 12, dependent on Claim 1, limits the system to one monitor input control signal, and one monitor output terminal during debug. The APA teaches the input control signal and output terminal, where in the Background (paragraph [0008]), the applicant describes a scan chain input control and output monitoring which is commonly known in the art as a JTAG interface, in which the input control and output (TMS, TDO) of a JTAG interface are commonly applied signals. And in view of the motivation previously stated, the claim is rejected.

5. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (herein "APA") published as U.S. Patent Application No. 2002/0026553, in view of Higashida, U.S. Patent No. 6523136, and in view of Ogino et

al., U.S. Patent No. 5416919 as applied to Claims 1 and 3, and further in view of Tashiro et al., U.S. Patent No. 5566303.

As per Claims 5 and 6:

Claims 5 and 6 further limit the claims to multiple processor units on the LSI circuit according to Claim 3, including multiple selection units, control signals, debug units, control circuits, as well as the external monitor control signal. Higashida in the dependent claims above teaches all of this, but does not teach multiple processors. Tashiro et al. does teach multiple processors (see FIG. 11 and 12) in column 1 lines 9-16. One with ordinary skill in the art at the time of the invention, motivated to providing test capabilities to all processors resident on a chip, as suggested by Tashiro et al. (see Abstract), would combine the processors of Tashiro et al. with the system configuration of Higashida, therefore the Claims 5 and 6 are rejected.

As per Claim 7:

Claim 7, dependent on Claim 5, limits the system to a serial to parallel converter for outputting to the outside. Higashida does output an 8-bit signal (see FIG.1 12), and therefore by virtue of the output bus size, does not require a serial/parallel conversion. If one were required, then as suggested for larger bus widths in column 8 lines 18-29 of Higashida, one would utilize a serial/parallel converter; and in view of the motivation previously stated, Claim 7 is rejected.

As per Claim 8:

Claim 8, dependent on Claim 5, limits the system to a parallel to serial converter for outputting to the outside. Higashida does output an 8-bit signal (see FIG.1 12), and

would therefore require a parallel/serial conversion. One with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and one monitor pin, and would require a standard parallel/serial converter. And in view of the motivation previously stated, Claim 8 is rejected.

As per Claim 9:

Claim 9, dependent on Claim 5 above, further limits the system to use of a thinning-out circuit. Higashida, in column 11 lines 56-67, column 12 lines 1-67, and column 13 lines 1-32, describes the use of flip-flops in-line with monitor data, triggered by a clock. As suggested by column 15, lines 1-6, the examiner recognizes the arrangement of flip-flops to be also a thinning-out circuit, however Higashida does not specify it as such. One with ordinary skill in the art at the time of the invention, motivated to reducing bandwidth of output data would be inclined to change the clock speed of the Higashida invention in order to thin out the signal, therefore the Claim 9 is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
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